1. A method of forming a semiconductor device on a semiconductor substrate, comprising the steps of:

forming a gate dielectric layer on said semiconductor substrate;

forming a conductive gate structure on a first area of said gate dielectric layer;

forming first insulator spacers on the sides of said conductive gate structure with the procedure used to form said first insulator spacers also removing a second area of said gate dielectric layer, wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers;

forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure of by said first insulator spacers;

forming second insulator spacers on the sides of said first insulator spacers; and

forming a second doped region in an area of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers.

2. The method of claim 1, wherein said gate dielectric layer is comprised of a layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide and silicon oxide.

3. The method of claim 1, wherein the thickness of said gate dielectric layer is between about 10 to 200 Angstroms.

4. The method of claim 1, wherein the dielectric constant of said gate dielectric layer is greater than 4.

5. The method of claim 1, wherein said conductive gate structure is comprised of doped polysilicon, at a thickness between about 300 to 3000 Angstroms.

6. The method of claim 1, wherein said conductive gate structure is comprised of metal silicide such as tungsten silicide.

7. The method of claim 1, wherein said first insulator spacers are comprised of silicon oxide, at a thickness between about 10 to 300 Angstroms.

8. The method of claim 1, wherein said first insulator spacers are comprised of silicon nitride, at a thickness between about 30 to 400 Angstroms.

9. The method of claim 1, wherein procedure used to define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said gate dielectric layer, is an anisotropic RIE procedure performed using Ar/CF_4 as a selective etchant for said first insulator spacer and for said gate dielectric layer.

10. A method of forming a semiconductor device on a semiconductor substrate featuring a high dielectric constant (high k), gate insulator layer, comprising the steps of:

forming said high k gate insulator layer on said semiconductor substrate;

forming a conductive gate structure overlying a first area of said high k gate insulator layer;

depositing an insulator layer;

performing a dry etch procedure to first define first insulator spacers on the sides of said conductive gate structure via etching of said insulator layer, and then to remove exposed portions of said high gate dielectric layer, wherein said exposed portions of said high k gate insulator layer are portions not covered by said conductive gate structure or by said first insulator spacers;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure of by said first insulator spacers;

forming second insulator spacers on the sides of said first insulator spacers; and

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers.

11. The method of claim 10, wherein said high k gate insulator layer is layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, and silicon oxide.

12. The method of claim 10, wherein the thickness of said high k gate insulator layer is between about 10 to 200 Angstroms.

13. The method of claim 10, wherein the dielectric constant of said high k gate insulator layer is greater than 4.

14. The method of claim 10, wherein said conductive gate structure is comprised of doped polysilicon, at a thickness between about 300 to 3000 Angstroms.

15. The method of claim 10, wherein said conductive gate structure is comprised of tungsten silicide.

16. The method of claim 10, wherein said insulator layer is selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

17. The method of claim 10, wherein the thickness of said insulator layer is between about 30 to 500 Angstroms.

18. The method of claim 10, wherein procedure used to both define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said high k gate insulator layer, is an anisotropic RIE procedure performed using Ar/CF_4 as a selective etchant for said insulator layer and for said high k gate insulator

19. A MOSFET device structure comprising:

a high dielectric constant (high k) gate insulator layer on a portion of a top surface of a semiconductor substrate;

a conductive gate structure on a first portion of said high k gate insulator layer;

first insulator spacers on sides of said conductive gate structure and overlying second portions of said high k gate insulator layer;

second insulator spacers on sides of said first insulator spacers and on sides of said second portions of said high k gate insulator layer;

a first doped region in a portion of said semiconductor substrate not covered by said conductive gate structure or by second portions of said high k gate insulator layer; and

a second doped region in a portion of said semiconductor substrate not covered by said conductive gate structure, by said second portions of said high k gate insulator layer, and by said second insulator spacers.

20. The MOSFET device structure of claim 19, wherein said high k gate insulator layer is selected from a group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, and silicon oxide.

21. The MOSFET device structure of claim 19, wherein the thickness of said high k gate insulator layer is between about 10 to 200 Angstroms.

22. The MOSFET device structure of claim 19, wherein the dielectric constant of said high k gate insulator layer is greater than 4.

23. The MOSFET device structure of claim 19, wherein said conductive gate structure is comprised of doped polysilicon or tungsten silicide, at a thickness between about 300 to 3000 Angstroms.

24. The MOSFET device structure of claim 19, wherein said first insulator spacers are selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

25. The MOSFET device structure of claim 19, wherein the thickness of said first insulator spacers is between about 30 to 500 Angstroms.

26. The MOSFET device structure of claim 19, wherein said second insulator spacers are comprised of silicon oxide or silicon nitride, at a thickness between about 200 to 1200 Angstroms.

27. The MOSFET device structure of claim 19, wherein said first doped region is a lightly doped source/drain region.

28. The MOSFET device structure of claim 19, wherein said second doped region is a heavily doped source/drain region.